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THERMAL STUDY OF THE DC BEHAVIOR IN $SIO_2/AL_{0.26}GA_{0.74}N/$ GAN MOS-HEMT

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ABSTRACT

In this work, we investigate the temperature-dependent DC behavior of an $Al_{0.26}Ga_{0.74}N/GaN$ Metal-Oxide-Semiconductor High Electron Mobility Transistors (MOS-HEMTs) using SiO_2 as gate oxide. A two dimensional numerical simulations is performed to describe thermal effect on the MOS-HEMT and the significant physics in the characteristics for $SiO_2/Al_{0.26}Ga_{0.74}N/GaN$ MOS-HEMT with gate length and source to drain spacing of 2 µm and 6 µm respectively. The corresponding drain current density with thermal effect in the 2 µm gate length MOS-HEMT is 390 mA/mm at the gate bias of 1.0 V. The thermal numerical model is also used to determine the distribution of the temperature with the drain-source and gate-source voltage. For Vgs = 0 V, a large global device temperature is observed when Vds is greater than 1 V. Furthermore, temperature and negative differential resistance are reduced during high-temperature operation.

KEYWORDS: $Al_{0.26}Ga_{0.74}N/GaN$, MOS-HEMT, SiO_2, Thermal, Temperature, Finite element

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Original Article

INTRODUCTION

High Electron Mobility Transistors (HEMTs) based on gallium nitride (GaN) is great candidate in the field of high-power, high frequencies and high temperature applications than other III-V HEMT due to their important parameters such as very high breakdown voltages and high sheet carrier densities [1, 2]. Unfortunately, the performance and reliability of the HEMT based on GaN is limited by high gate leakage current due to the surface de-fects and finite barrier height [3, 4, 5]. In order to improve reverse blocking characteristics, many significant research groups attempted to suppress the gate leakage by using the metal-oxide-semiconductor field-effect transistor (MOSFET) approaches using SiO_2[6,7], Si_3N_4 [8,9], Al_2O_3 [10, 11] and other oxides. Further improvement of III-nitride MOS-HEMT performance results from high-quality insulating materials/AlGaN interface. Furthermore, since the dielectric constant of Al2O3 is greater than twice that of SiO2 for a given gate voltage a MOS-HEMT made with a high-k gate will result in a larger inversion charge. Generally, the MOS-HEMT offer low gate leakage currents for a larger voltage swing and better device reliability. Adivarahan reported a MOS-HEMT with an output power density of 18.6 W/mm and a PAE of 49.5% at a drain bias of 55 V at 2 GHz [12].

Also, the performance of the transistor MOS-HEMT is influenced by the temperature and consequently by the self-heating effect. This effect occurs usually when the transistor operates at high drain-source voltage There are a few work reported in the literature on the thermal effect on the characteristics of the MOS-HEMT, for example, the self-heating of GaN-based metal-oxide-semiconductor high-electron-mobility transistors including hot

electron and quantum effects is simulated by [13], the temperature-dependent characteristics of AlGaN/GaN MOS-HEMT by using hydrogen peroxide oxidation technique is investigated by [14] and the thermal stability of AlGaN/GaN MOS-HEMTs using Gd2O3 as gate dielectric is studied by [15].

The purpose of this work is to investigate the heat conduction effect on the DC characteristics of 2 µm SiO_2/AlGaN/GaN MOS-HEMT transistor. The device structure was analysed and simulated using the software package ATLAS, from Silvaco [16]. We developed an electro-thermal model by coupling the drift diffusion carrier transport model and the heat conduction equation. Different electronic properties such as the mobility of carriers, the velocity and the thermal conductivity of the SiO_2/$Al_{0.26}Ga_{0.74}N$/GaN HEMT were introduced in our numerical model.

Temperature Dependent Parameters of Sio_2/$Al_{0.3}ga_{0.7}n$/Gan Mos-Hemt

In SiO_2/$Al_{0.3}Ga_{0.7}N$/GaN MOS-HEMT transistor there are different factors dependent temperature such as the energy band gap, the electron mobility, the saturation velocity and the thermal conductivity.

For GaN, the band gap energy is calculated using [17]:

$$E_g = 3.507 - \frac{0.909.10^{-3}.T^2}{T + 830.0} \tag{1}$$

For $Al_xGa_{1-x}N$ the dependence on composition fraction, x, with the band gap energy, is described by:

$$E_g = E_g(AlN)x + E_g(GaN)(1-x) - 1.3(1-x) \tag{2}$$

The electron mobility is calculated by (3) in both the AlGaN and GaN [18]:

$$\mu(E) = \mu_0(T_L)\left[\frac{1}{1+\left(\frac{\mu_0 E}{v_{sat}}\right)^{\beta}}\right]^{1/\beta} \tag{3}$$

Where $\mu_0(T_L)$ is the mobility at low electric field and the quoted β is often equal to 2.

The temperature variation of saturation velocity is expressed by:

$$v_{sat}(T) = \frac{\alpha}{1+\theta\exp\left(\frac{T_L}{600}\right)} \tag{4}$$

The values of α and θ are respectively 4.6 10^7 cm/s and 0.8 [19].

The variation of the thermal conductivity with temperature in both GaN and AlGaN is calculated by the following equation [16]:

$$K(T) = k(300)\left(\frac{T_L}{300}\right)^{\alpha} \tag{5}$$

For GaN, k(300) = 1.30 W/cm K and α = -0.28 [17]. For $Al_{0.3}Ga_{0.7}N$, k(300) = 0.13 W/cm K.

For SiO_2, the thermal conductivity is almost 0.014 W/cm K

The details of the MOS-HEMT structure and DC performance with thermal effect will be explained in the following section.

MOS-HEMT SIMULATED RESULT AND DISCUSSIONS

Figure 1 shows the schematic cross section of the $SiO_2/Al_{0.3}Ga_{0.7}N/GaN$ MOS-HEMT structure from Atlas, this simulator has been widely used by researchers in universities and also in industry. the gate length of simulated MOS-HEMT is 2 µm, this structure consists of sapphire substrate, an GaN buffer layer with a thickness of 2,23 µm, an undoped GaN channel layer with a thickness of 50 nm, and an undoped 25 nm AlGaN barrier layer with an Al composition of 0,26. An electron sheet density of $4{,}3.10^{12}$ cm^{-2} was specified. The gate-source and the gate-drain spacing are 2 µm.

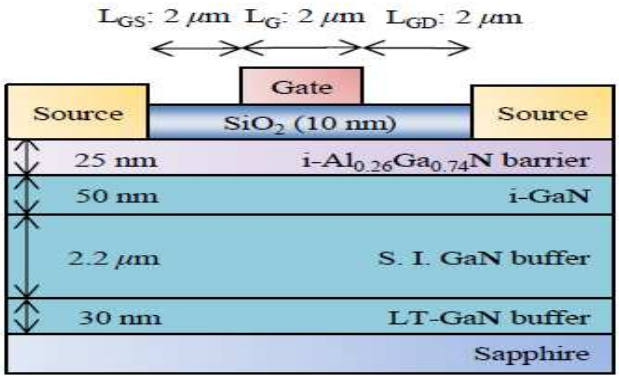
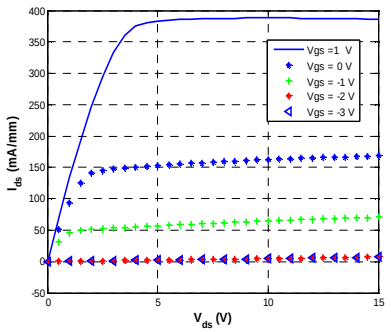


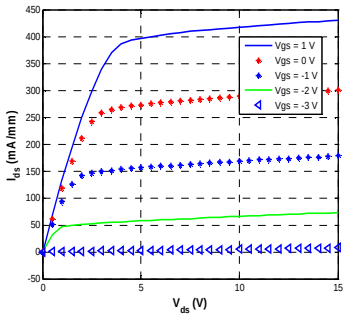
Figure 1: Cross Section Simulated $Al_{0.3}Ga_{0.7}N/GaN$ MOS-HEMT [5]

Figure 2a and 2b depicts respectively our simulated thermal and isothermal output Ids-Vds characteristics of an MOS-HEMT with a gate length and width respectively of 2 µm and 100 µm at lattice temperature, the gate voltage varies from 1 to -3 V with steps of -1 V.

As seen in Figures 2a and 2b, with thermal effect, the drain current decreases, which increases the device lattice temperature and consequently reduces physical parameters such as mobility and carrier saturation velocity. We note also that the negative differential conductance suppressed for this structure. At room temperature, the device exhibited a saturated drain current (Ids) respectively of 390 mA/mm and 425 mA/mm with thermal and isothermal calibration. For same bias condition of Vds (Vds = 10 V), there is almost 8,23 percent degradation of current due to heat conduction effects for Vgs = 1 V and almost 50 percent for Vgs = 0 V. In general, we have achieved a very good agreement between isothermal simulation and measurement Ids-Vds characteristics of [5].



a MOS-HEMT Simulated Thermal Ids-Vds Characteristics at T = 300 K.



b MOS-HEMT simulated Isothermal Ids-Vds Characteristics at T = 300 K.

Figure 2: MOS-*HEMT Ids-Vds Characteristics.*

The simulated thermal transfer characteristics of the $Al_{0.26}Ga_{0.74}N$/GaN MOS-HEMT at lattice temperature in the linear region (solid line) and in the saturation region (symbol line) are plotted in Figure 3, the drain-source voltage is fixed to 5 and 1 V. From Figure 3, the threshold voltage is of a –3 V at room temperature for the saturation region. The threshold voltage of the MOS-HEMTs shifted to more negative values relative to the HEMTs because of the longer gate-to-channel separation with additional SiO_2 under the gate contact.

In order to investigate the distribution of the temperature in the MOS-HEMT and conventional HEMT, Figure 4a and Figure 4b depicts the variations of the global devices temperature for the thermal model with the applied drain bias as a function of the gate bias (Vgs = 0 and - 2 V). As shown in Figure 4a and Figure 4b, we note that at low drain voltages the global device temperature is close to the lattice temperature. Indeed, a large temperature device is observed when the drain voltage is greater than 1 V and 3 V for Vgs = 0 V and -2 V respectively due to the existence of a high electric field in the gate-to-drain region.

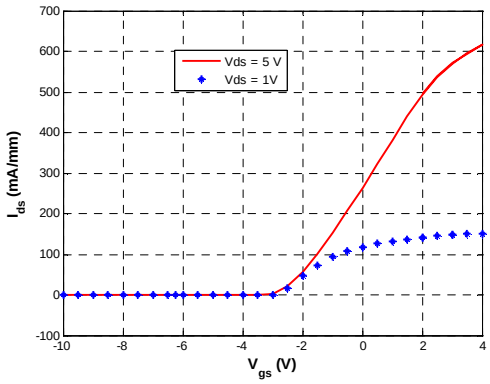
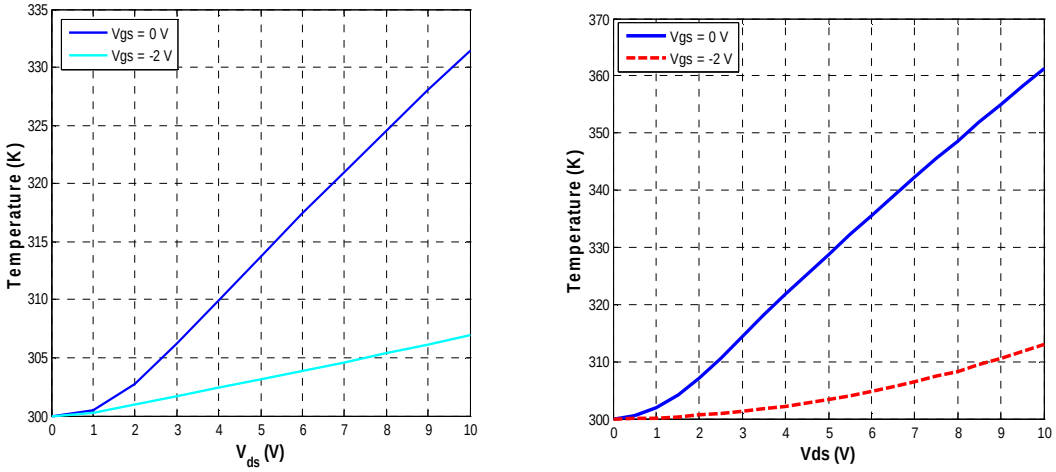


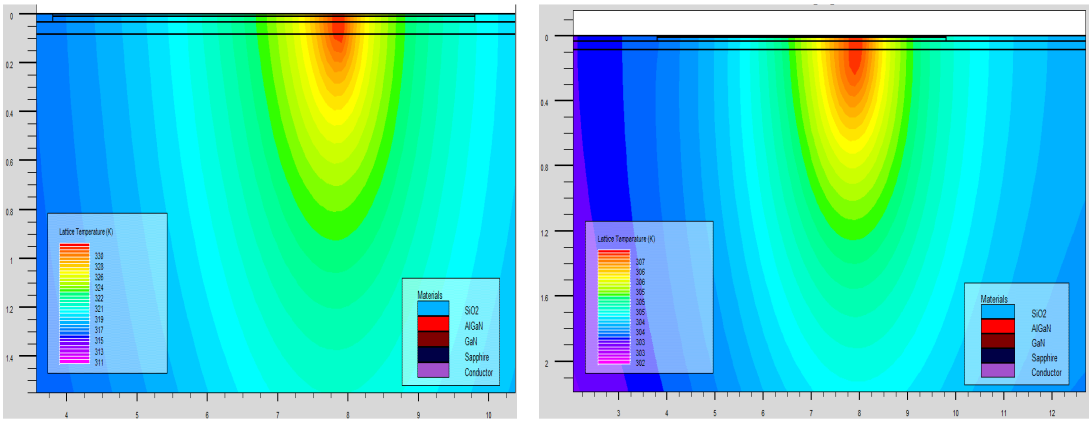
Figure 3: MOS-HEMT Thermal Transfer Characteristics at T = 300 K, Vds = 1 and 5 V

Figure 5a and Figure 5b show the temperature contour from thermal simulations of MOS-HEMT at biases points of gate voltage of 0 V and -2 V and the drain voltage of 10 V. As seen in Figure 5a and Figure 5b the obtained peak temperature in the hot spot is almost 360 K and 313 K for Vgs = 0 V and Vgs = -2 V respectively. Indeed, the existence and the spread of the hot spot region centered at the drain end of the barrier with increasing of gate voltage.



a. MOS-HEMT Transistor **b HEMT Transistor [20]**

Figure 4: Global Device Temperature for Vgs = 0V and -2 V



a. Vds = 10 V and Vgs = 0 V. **b. Vds = 10 V and Vgs = -2 V.**

Figure 5: Two-Dimensional $Al_{0.26}Ga_{0.74}N/GaN$ MOS-HEMT Temperature Distribution for

CONCLUSIONS

In this paper, the thermal behavior of the 2 µm gate length GaN MOS-HEMTs with an SiO_2 gate oxide grown on sapphire substrate is analysed and discussed under steady-state study. The degradations of the DC behavior and consequently the performances of the device have been observed due to the heat conduction effect. We note in particular that the gate and the drain voltage influence the device temperature distribution and especially the hot spot of the device. Also, for the same gate and drain polarisation (Vds = 10 V, Vgs = 0 V), the hot spot in MOS-HEMT is smaller than that conventional HEMT, these characteristics imply the huge potential of the SiO_2/AlGaN/GaN MOS-HEMT for high temperature applications.

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